MIC5162

Dual Regulator Controller For DDR2/3 Memory and High-Speed Bus Termination

General Description

The MIC5162 is a dual regulator controller designed for high-speed bus termination. It offers a simple, low-cost JEDEC compliant solution for terminating high-speed, low-voltage digital buses (i.e. DDR, DD2, DDR3, SCSI, GTL, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc).

The MIC5162 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET depending on whether the current is being sourced to the load or sinked by the regulator.

Designed to provide a universal solution for bus termination regardless of input voltage, output voltage, or load current, the desired MIC5162 output voltage can be programmed by externally forcing the reference voltage.

The MIC5162 operates from an input of 1.35V to 6V, with a second bias supply input required for operation. It is available in the tiny MSOP-10 package with operating junction temperature range of –40°C to +125°C.

Features

- JEDEC Compliant Bus Termination for SCSI, GTL, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc.
- DDR, DDR2, DDR3, memory termination
- Tracking programmable output
- Requires minimal external components
- Wide bandwidth
- Input voltage range: 1.35V to 6V
- Logic controlled enable input
- Tiny MSOP-10 package
- Available –40°C < T_J < +125°C

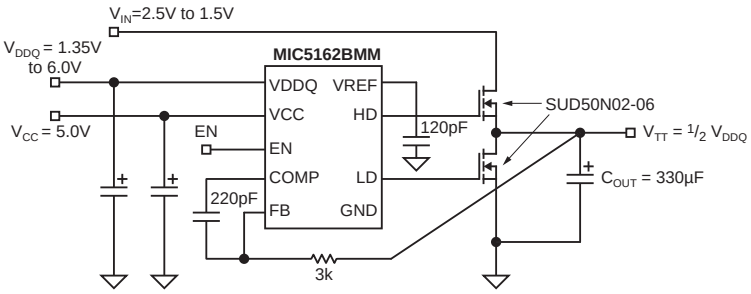
Applications

- Desktop computers
- Notebook computers
- Communication systems
- Video cards
- DDR/DDR2/DDR3 memory termination

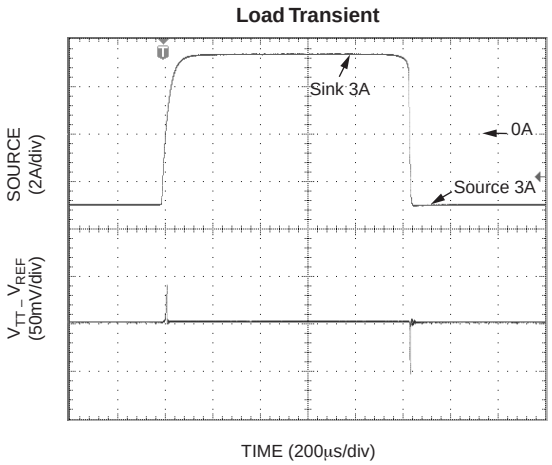
Ordering Information

Part Number	Junction Temp. Range	Package
MIC5162BMM	–40°C to +125°C	10-Pin MSOP

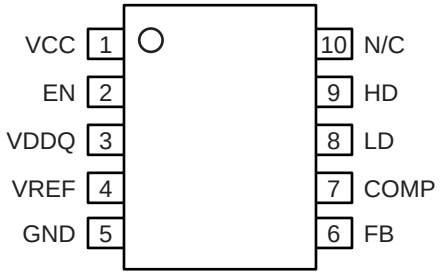
Typical Application



Typical SSTL-2 Application



Pin Configuration



10-Lead MSOP

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Bias Supply Input. Apply 5V to this input for internal bias to the controller.
2	EN	Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown.
3	VDDQ	Input supply voltage.
4	VREF	Reference output equal to half of V_{DDQ}.
5	GND	Ground.
6	FB	Feedback input to the to the internal error amplifier.
7	Comp	Compensation (Output): Connect a capacitor to feedback pin for compensation of the internal control loop.
8	LD	Low-side drive: Connects to the Gate of the external low side MOSFET.
9	HD	High-side drive: Connects to the Gate of the external high side MOSFET.
10	N/C	Not internally connected.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) 7V
Supply Voltage (V_{DDQ}) 7V
Enable Input Voltage (V_{EN}) 7V
Junction Temperature Range ..... $-40°C < T_J < +125°C$

Operating Ratings (Note 2)

Supply Voltage (V_{CC}) ..... 3V to 6V
Supply Voltage (V_{DDQ}) ..... 1.35V - 6V
Enable Input Voltage (V_{EN}) ..... 0V to VIN

Electrical Characteristics

T_A = 25°C with V_{DDQ} = 2.5V; V_{CC} = 5V; V_{EN} = V_{CC}; **bold** values indicate –40ºC<T_J<+125ºC; unless otherwise specified. See test circuit 1 for test circuit configuration.

Parameter	Condition	Min	Typ	Max	Units
V_{REF} Voltage		–1%	0.5V_{DDQ}	1%	V
V_{TT} Voltage Accuracy (Note 2)	Sourcing; 100mA to 3A	–5 **–10**	0.4	5 **–10**	mV
	Sinking; –100mA to –3A	–5 **–10**	0.6	5 **10**	mV
Supply Current (I_{DDQ})	V_{EN} = 1.2V (controller ON) No Load		120	140 **200**	µA
Supply Current (I_{CC})	No Load		15	20 **25**	mA
I_{CC} Shutdown Current (Note 3)	V_{EN} = 0.2V (controller OFF)		10	**35**	µA
Start–up Time (Note 4)	V_{CC}, = 5V external bias; V_{EN} = V_{IN}		8	15 **30**	µs
Enable Input					
Enable Input Threshold	Regulator enable	**1.2**			V
	Regulator shutdown			**0.3**	V
Enable Hysteresis			40		mV
Enable Pin Input Current	V_{IL} < 0.2V (controller shutdown)		0.01		µA
	V_{IH} > 1.2V (controller enabled)		5.5		µA
Drive					
High Side Gate Drive Voltage	High Side MOSFET Fully ON	**4.8**	4.97		V
High Side Gate Drive Voltage	High Side MOSFET Fully OFF		0.03	**0.2**	V
Low Side Gate Drive Voltage	Low Side MOSFET Fully ON	**4.8**	4.97		V
Low Side Gate Drive Voltage	Low Side MOSFET Fully OFF		0.03	**0.2**	V

Note 1. Exceeding the absolute maximum ratings may damage the device.

Note 2. The V_{TT} voltage accuracy is measured as a delta voltage from the reference output ($V_{TT} – V_{REF}$).

Note 3. Shutdown current is measured only on the V_{CC} pin. The V_{DDQ} pin will always draw a minimum amount of current when voltage is applied.

Note 4. Start-up time is defined as the amount of time from V_{EN} = V_{CC} to HSD = 90% of V_{CC}.

Test Circuit

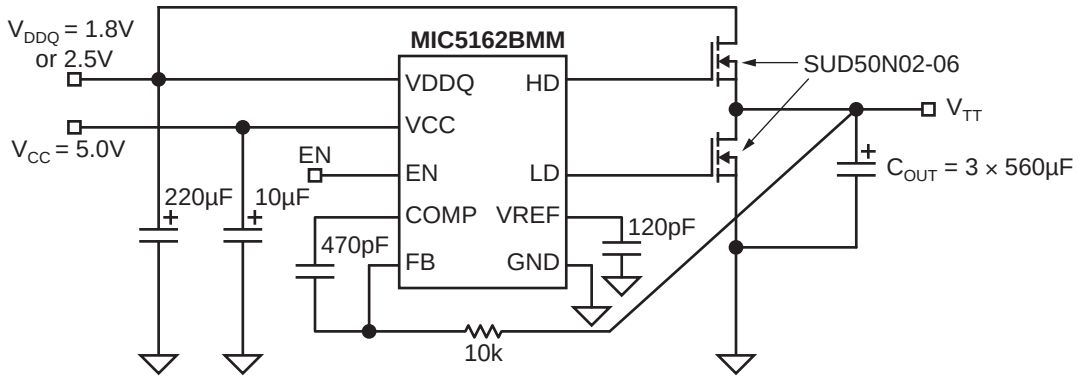
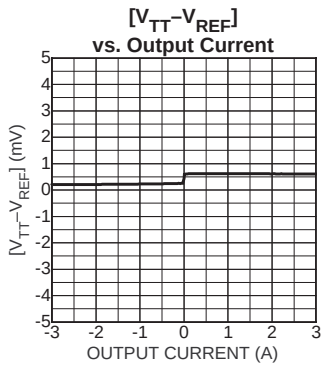
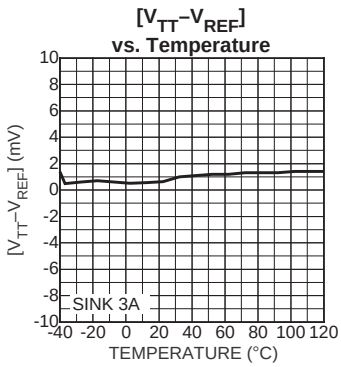
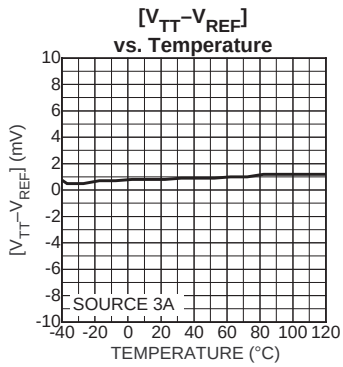


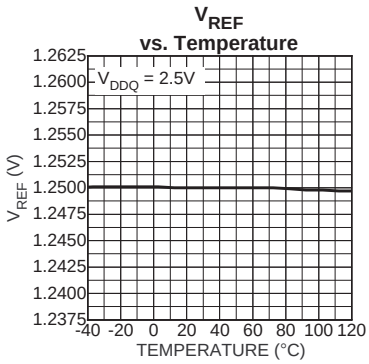
Figure 1. Test Circuit

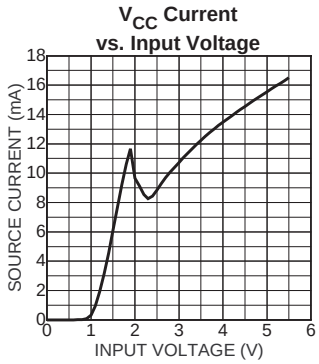
Typical Characteristics

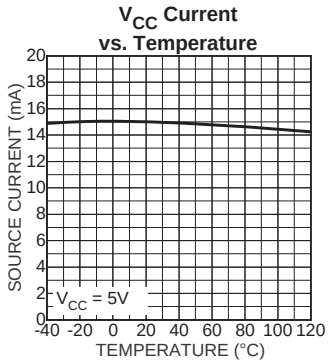




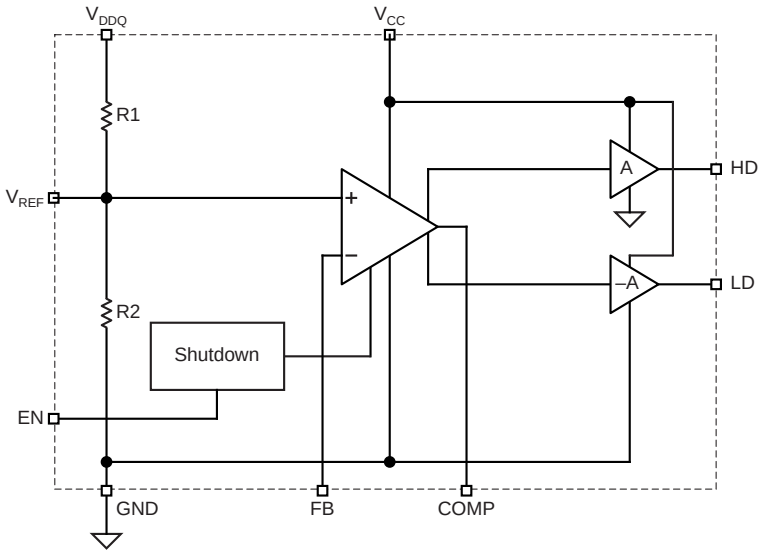








Functional Diagram



Block Diagram

Applications Information

High performance memory requires high speed signaling. This increase in speed requires special attention to maintain signal integrity. Bus termination provides a means to increase signaling speed while maintaining good signal integrity. An example of bus termination is the Series Stub Termination Logic or SSTL. Figure 1 is an example of an SSTL 2 single ended series parallel terminated output. SSTL 2 is a JEDEC signaling standard operating off of a 2.5V supply. It consists of a series resistor (R_S) and a terminating resistor (R_T). Values of R_S will range between 10Ω to 30Ω with a typical of 22Ω, while R_T will range from 22Ω to 28Ω with a typical value of 25Ω. V_{REF} must maintain 1/2 V_{DD} with a ±1% tolerance, while V_{TT} will dynamically sink and source current to maintain a termination voltage of ±40mV from the V_{REF} line under all conditions. This method of bus termination reduces common mode noise, settling time, voltage swings, EMI/RFI and improves slew rates.

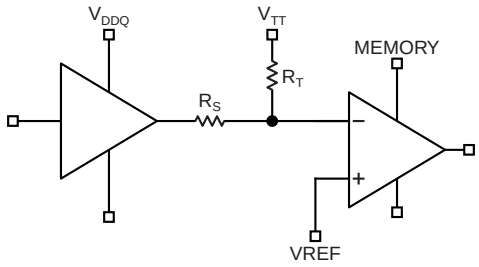


Figure 1.

The MIC5162 is a high performance linear controller, utilizing scalable N-Channel MOSFETs to provide JEDEC compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage by half, providing the reference (V_{REF}) voltage. An internal error amplifier compares the termination voltage (V_{TT}) and V_{REF}, controlling 2 external N-Channel MOSFETs to sink and/or source current to maintain a termination voltage (V_{TT}) equal to V_{REF}. The N-Channels receive their enhancement voltage from a separate V_{CC} pin on the device.

Although the general discussion is focused on SSTL, the MIC5162 is also capable of providing bus terminations for SCSI, GTL, HSTL, LV-TTL, Rambus, LV-PECL and other systems.

V_{DDQ}

The V_{DDQ} pin on the MIC5162 provides the source current through the high side N-Channel and the reference voltage to the device. The MIC5162 can operate at V_{DDQ} voltages as low as 1.35V. Due to the possibility of large transient currents being sourced from this line, significant bypass capacitance will aid in performance by improving the source impedance at higher frequencies. Since the reference is simply $V_{DDQ}/2$, perturbations on the V_{DDQ} will also appear at half the amplitude on the reference. For this reason, low ESR capacitors such as ceramics or Oscons are recommended on V_{DDQ}.

V_{TT}

V_{TT} is the actual termination point. V_{TT} is regulated to V_{REF}. Due to high speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate large signal transient response, large Oscons ceramics are recommended on V_{TT}. The proper combination and placement of the Oscon and ceramic capacitors is important to reduce both ESR and ESL such that high-current high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The larger Oscon capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is typically important to reduce the effects of PCB trace inductance.

V_{REF}

Two resistors dividing down the V_{DDQ} voltage provide V_{REF} (Figure 3). The resistors are valued at around 17kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is required to remove high frequency signals reflected from the source. Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down V_{REF} and detract from the reference voltage's ability to track V_{DDQ} during high speed load transients.

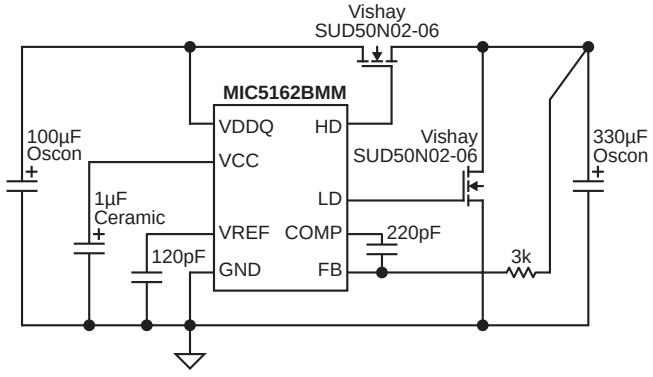


Figure 2.

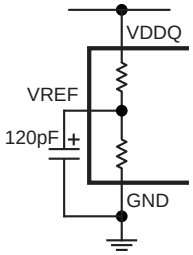


Figure 3.

V_{REF} can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistors can be added from V_{REF} to ground or V_{REF} to V_{DDQ} to shift the reference point up or down.

V_{CC}

V_{CC} supplies the internal circuitry of the MIC5162 and provides the drive voltage to enhance the external N-Channel MOSFETs. A small 1μF capacitor is recommended for bypassing the V_{CC} pin. The minimum V_{CC} voltage should be a gate-source voltage above V_{TT} without exceeding 6V. For example, on an SSTL compliant terminator, V_{DDQ} equals 2.5V and V_{TT} equals 1.25V. If the N-Channel MOSFET selected requires a gate source voltage of 2.5V, V_{CC} should be a minimum of 3.75V.

Feedback and Compensation

The feedback provides the path for the error amplifier to regulate V_{TT}. An external resistor must be placed between the feedback and V_{TT}. This allows the error amplifier to be correctly externally compensated.

For most applications, a 3kΩ resistor is recommended.

The COMP pin on the MIC5162 is the output of the internal error amplifier. By placing a capacitor between the COMP pin and the feedback pin, this coupled with the feedback resistor places an external pole on the error amplifier. With a 3kΩ feedback resistor, a minimum 220pF capacitor is recommended for a 3A peak termination circuit. Increases in load, multiple N-Channel MOSFETs and/or increase in output capacitance may require feedback and/or compensation capacitor values to be increased to maintain stability. Feedback resistor values should not exceed 100kΩ and compensation capacitors should not be less than 40pF.

Enable

The MIC5162 features an active high enable input. In the off mode state, leakage currents are reduced to microamperes. The enable input has thresholds compatible with TTL/CMOS for simple logic interfacing. The enable pin can be tied directly to V_{DDQ} or V_{CC} for functionality. Do not float the enable pin. Floating this pin causes the enable to be in an indeterminate state.

Input Capacitance

Although the MIC5162 does not require an input capacitor for stability, using one greatly improves device performance. Due to the high-speed nature of the MIC5162, low ESR capacitors such as Oscon and ceramics are recommended for bypassing the input. The recommended value of capacitance will depend greatly on the proximity to the bulk capacitance. Although a 10μF ceramic capacitor will suffice for most applications, input capacitance may need to be increased in cases where the termination circuit is greater than 1" away from the bulk capacitance.

Output Capacitance

Large, low ESR capacitors are recommended for the output (V_{TT}) of the MIC5162. Although low ESR capacitors are not required for stability, they are recommended to reduce the effects of high-speed current transients on V_{TT}. The change in voltage during the transient condition will be the effect of the peak current multiplied by the output capacitor's ESR. For that reason, Oscon type capacitors are excellent for this application. They have extremely low ESR and large capacitance-to-size ratio. Ceramic capacitors are also well suited to termination due to their low ESR. These capacitors should have a dielectric rating of X5R or X7R. Y5V and Z5U type capacitors are not recommended, due to their poor performance at high frequencies and over temperature. The minimum recommended capacitance for a 3 amp peak circuit is 100μF. Output capacitance can be increased to achieve greater transient performance.

MOSFET Selection

The MIC5162 utilizes external N-Channel MOSFETs to sink and source current. MOSFET selection will settle to two main categories: size and gate threshold (V_{GS}).

MOSFET Power Requirements

One of the most important factors is to determine the amount of power the MOSFET is going to be required to dissipate. Power dissipation in an SSTL circuit will be identical for both the high side and low side MOSFETs. Since the supply voltage is divided by half to supply V_{TT}, both MOSFETs have the same voltage dropped across them. They are also required to be able to sink and source the same amount of current (for either all 0's or all 1's). This equates to each side being able to dissipate the same amount of power. Power dissipation calculation for the high-side driver is as follows:

$$P_D = \left(V_{DDQ} - V_{TT}\right) \times I\_SOURCE$$

Where I_source is the average source current.

Power dissipation for the low-side MOSFET is as follows;

$$P_D = V_{TT} \times I\_SINK$$

Where I_sink is the average sink current.

In a typical 3 amp peak SSTL_2 circuit, power considerations for MOSFET selection would occur as follows.

$$P_D = \left(V_{DDQ} - V_{TT}\right) \times I\_SOURCE$$

$$P_D = \left(2.5V - 1.25V\right) \times 1.6A$$

$$P_D = 2W$$

This typical SSTL_2 application would require both high-side and low-side N-Channel MOSFETs to be able to handle 2 Watts each. In applications where there is excessive power dissipation, multiple N-Channel MOSFETs may be placed in parallel. These MOSFETs will share current, distributing power dissipation across each device.

The maximum MOSFET die (junction) temperature limits maximum power dissipation. The ability of the device to dissipate heat away from the junction is specified by the junction-to-ambient (θ_{JA}) thermal resistance. This is the sum of junction-to-case (θ_{JC}) thermal resistance, case-to-sink (θ_{CA}) thermal resistance and sink-to-ambient (θ_{SA}) thermal resistance;

$$\boldsymbol{\theta}_{JA} = \boldsymbol{\theta}_{JC} + \boldsymbol{\theta}_{CS} + \boldsymbol{\theta}_{SA}$$

In our example of a 3A peak SSTL_2 termination circuit, we have selected a D-pack N-Channel MOSFET that has a maximum junction temperature of 150°C. The device has a junction-to-case thermal resistance of 1.5°C/Watt. Our application has a maximum ambient temperature of 60°C. The required junction-to-ambient thermal resistance can be calculated as follows;

$$\boldsymbol{\theta}_{JA} = \frac{T_J - T_A}{P_D}$$

Where T_J is the maximum junction temperature, T_A is the maximum ambient temperature and P_D is the power dissipation.

In our example;

$$\boldsymbol{\theta}_{JA} = \frac{T_J - T_A}{P_D}$$

$$\boldsymbol{\theta}_{JA} = \frac{150°C - 60°C}{2W}$$

$$\boldsymbol{\theta}_{JA} = 45°C/W$$

This shows that our total thermal resistance must be better than 45°C/W. Since the total thermal resistance is a combination of all the individual thermal resistances, the amount of heat sink required can be calculated as follows;

$$\boldsymbol{\theta}_{SA} = \boldsymbol{\theta}_{JA} - \left(\boldsymbol{\theta}_{JC} + \boldsymbol{\theta}_{CA}\right)$$

In our example;

$$\boldsymbol{\theta}_{SA} = 45°C/W - \left(1.5°C/W + 0.5°C/W\right)$$

$$\boldsymbol{\theta}_{SA} = 43°C/W$$

In most cases, case-to-sink thermal resistance can be assumed to be about 0.5°C/W.

The SSTL termination circuit for our example, using 2 D-pack N-Channel MOSFETs (one high side and one on the low side) will require at least a 43°C/W heat sink per MOSFET. This may be accomplished with an external heat sink or even just the copper area that the MOSFET is soldered to. In some cases, airflow may also be required to reduce thermal resistance.

MOSFET Gate Threshold

N-Channel MOSFETs require an enhancement voltage greater than its source voltage. Typical N-Channel MOSFETs have a gate-source threshold (V_{GS}) of 1.8V and higher. Since the source of the high side N-Channel is connected to V_{TT}, the MIC5162 V_{CC} pin requires a voltage equal to or greater than the V_{GS} voltage. For example, our SSTL_2 termination circuit has a V_{TT} voltage of 1.25V. For an N-Channel that has a V_{GS} rating of 2.5V, the V_{CC} voltage can be as low as 3.75V. With an N-Channel that has a 4.5V V_{GS}, the minimum V_{CC} required is 5.75V. Although these N-Channels are driven below their full enhancement threshold, it is recommended that the V_{CC} voltage has enough margin to be able to fully enhance the MOSFETs for large signal transient response. In addition, low gate thresholds MOSFETs are recommended to reduce the V_{CC} requirements.

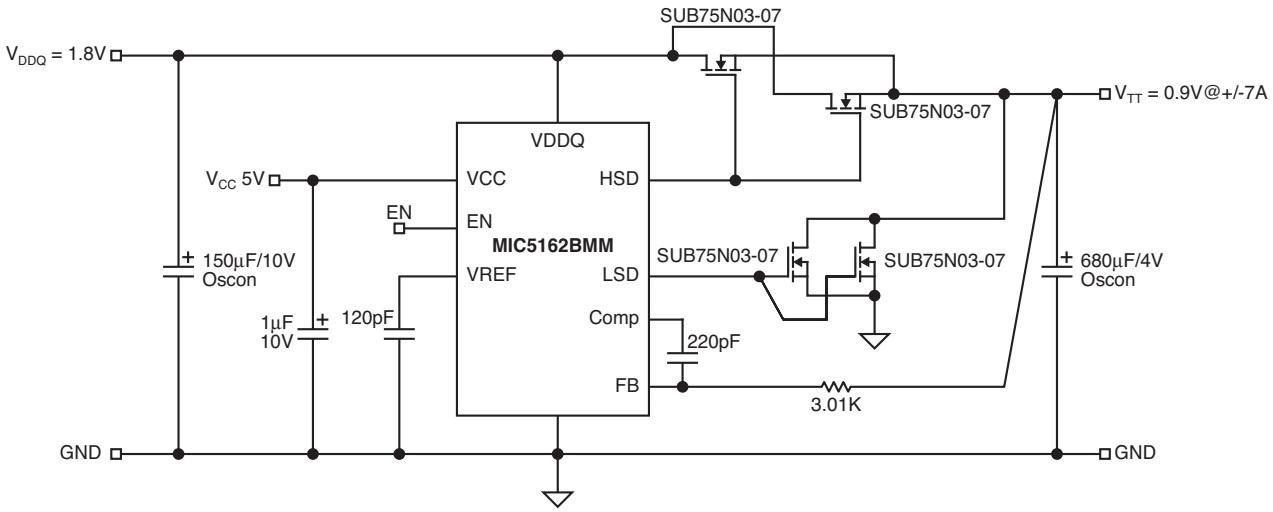
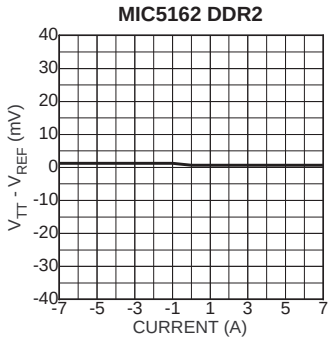
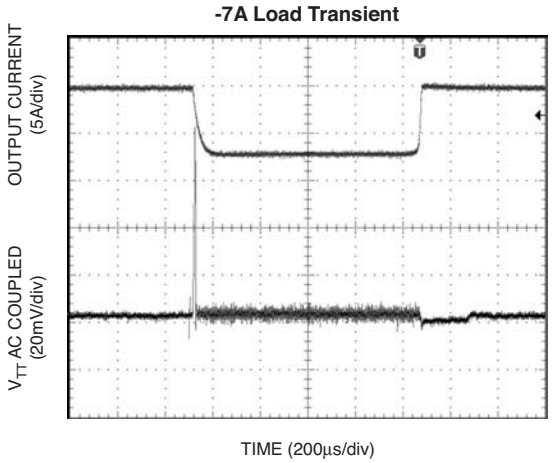
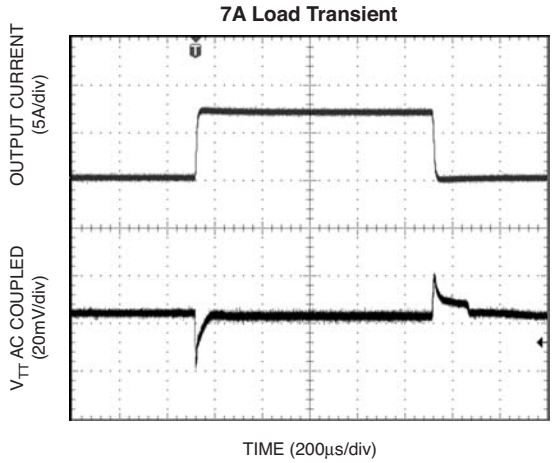


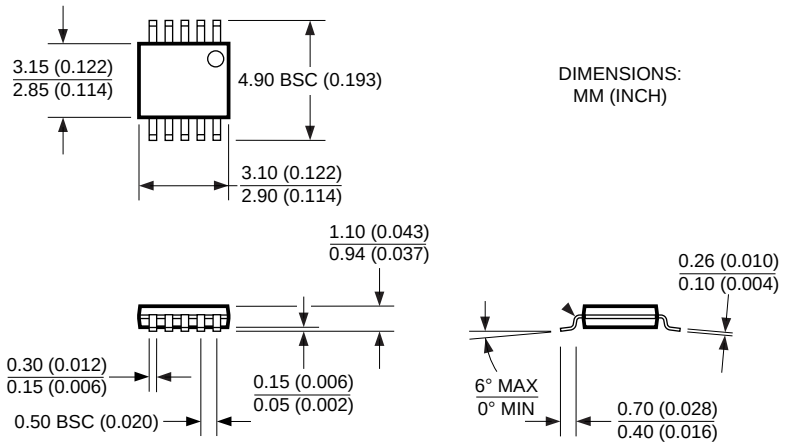
Figure 4. DDR2 Termination







Package Information



10-Pin MSOP (M)

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